APPLICATION FOR UNITED STATES LETTERS PATENT

of

Salvador Salcido, Jr.
32858 Fircreek Ln.
Philomath, Oregon 97370

Michael G. Kelly
3220 N.W. Buttercup Drive
Corvallis, Oregon 97330

Michael D. Cusack
12474 W. Sitka Drive
Boise, Idaho 83713

Ravindhar K. Kaw
1128 Machado Ln.
San Jose, California 95127

for

INTEGRATED CIRCUIT WITH COPPER INTERCONNECT AND TOP LEVEL BONDING/INTERCONNECT LAYER

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland CO 80537-0599

File No. 10030277-1

Certificate of Mailing Under 37 C.F.R. § 1.10

Express Mail Label No. EU 988425015 US Date of Deposit: October 3, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to:MS PATENT APPLICATION, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kelly Pedersen

Kelly Pedersen

INTEGRATED CIRCUIT WITH COPPER INTERCONNECT AND TOP LEVEL BONDING/INTERCONNECT LAYER

BACKGROUND OF THE INVENTION

[1] Integrated circuits with copper interconnects are devices well known in the art. Such devices include a semiconductor substrate having circuits formed therein by diffusion. Overlying the substrate is usually one or more copper interconnect layers separated by insulating layers. The copper interconnect layers are configured to distribute external signals and power and ground about the integrated circuit and are connected to the integrated circuit by vias in the insulating layer or layers.

[2] While such devices are used widely, it has been found that as circuit density increases, power delivery to the integrated circuits becomes increasingly difficult. This is at least partly due to die size, operating frequencies, and device leakage.

[3] Integrated circuits with copper interconnects also can suffer from delamination. This delamination may be due to a mismatch of expansion coefficients between the package overmold compound used in the devices and the metal interconnects.

[4] In the past, the above deficiencies have been addressed by the provision of wider metal interconnect tracks. This has also required additional power and ground cells to accommodate the wider metal interconnect tracks. Further, additional metal interconnect layers have been included in the devices. Still further, different molding compounds have been adapted for packaging the devices. Unfortunately, these measures are generally more expensive to employ.

[5] In integrated circuits employing copper interconnects, connectivity to the package is accomplished by transition vias to top surface aluminum bond pads. The bonding pads are used as bonding sites for wire bonding or a solder bump redistribution layer.

[6] The present invention provides an improved integrated circuit employing copper interconnects. The integrated circuit of the present invention provides protection against to copper interconnect delamination. It further provides power delivery to the devices with reduced resistance and increased reliability at reduced costs.

SUMMARY OF THE INVENTION

[7] In accordance with one aspect of the present invention, the present invention provides an integrated circuit assembly having a substrate of semiconductor material including a circuit integrally formed therein, an interconnection layer overlying the substrate and making selective electrical connection to the circuit integrally formed in the substrate, the interconnect layer being formed of a first conductive material, and a distribution layer overlying the interconnection layer and including wire bonding pads for wire bonding to selected electrical signals. The distribution layer may be formed of a second conductive material. It may further include distribution grids connected to the wire bonding pads and extend over the interconnection layer. The assembly further includes a plurality of connecting channels connecting selected ones of the distribution grids to selected locations of the interconnection layer.

[8] The first conductive material may be copper and the second conductive material may be aluminum. The selected locations of the interconnection layer may include power connections and at least one of the wire bonding pads may be coupled to the power connections. The selected locations of the interconnection layer may include ground connections and at least one of the wire bonding pads may be coupled to the ground connections. The connecting channels are preferably distributed throughout the distribution layer.

[9] In accordance with further aspects of the present invention, the assembly may further include a package having a surface including wire bonding pads. The substrate may be mounted on the package surface. Wire bonds may then couple the wire bonding pads of the package to the wire bonding pads of the distribution layer. The wire bonding pads of the package may include ground and power pads. The wire bonding pads may further be disposed at the periphery of the distribution layer. The distribution grids may be configured as a star pattern or alternatively an orthogonal grid pattern.

[10] In accordance with further aspects of the present invention, the invention provides an integrated circuit including a substrate of semiconductor material, a first metalization layer overlying the substrate, and an insulator layer overlaying the metalization layer and including a plurality of vias. The integrated circuit further includes a second metalization layer overlying the insulator layer and making selective contact with the first metalization layer through the vias. The second metalization layer includes wire bonding pads and distribution grids coupled to the bonding pads. The distribution grids are distributed over the insulator layer.

[11] The first metalization layer may be a copper interconnection layer and the second metalization layer may be an aluminum distribution layer. The integrated circuit may further include a package supporting the substrate and including ground and power bonding pads wire bonded to the wire bonding pads.

BRIEF DESCRIPTION OF THE DRAWINGS

[12] The foregoing aspects and many of the attended advantages of this invention will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[13] **FIG. 1** is a side view of an integrated circuit assembly embodying the present invention including a processed semiconductor substrate mounted on its integrated circuit package;

[14] **FIG. 2** is a top view of the processed integrated circuit substrate of **FIG. 1**; and

[15] **FIG. 3** is a top view of another processed integrated circuit substrate embodying the present invention.

DESCRIPTION OF THE INVENTION

[16] Referring now to **FIG. 1**, it shows an integrated circuit assembly ***10*** embodying the present invention. The assembly ***10*** includes a processed semiconductor substrate ***12***, an interconnect layer ***14***, an insulator layer ***16***, and a distribution layer ***18***. The processed semiconductor substrate ***12*** is mounted on an integrated circuit package ***20***.

[17] The semiconductor substrate ***12*** has been processed to include an integrated circuit ***22*** diffused therein. The integrated circuit ***22*** may be formed in the substrate ***12*** using diffusion and masking techniques well known in the art.

[18] The interconnect layer ***14*** is formed of a first conductor such as, for example, copper. The copper interconnection layer ***14*** overlies the substrate ***12*** and selectively makes electrical connection to the circuit ***22*** integrally formed in this substrate in a manner well known in the art. As is well known in the art, the interconnection layer ***14*** may make selective electroconnection to the circuit ***22*** through vias formed in an intervening insulative layer. Further, the interconnection layer may comprise a plurality of interspersed conductive layer patterns and oxide layers as are also known in the art.

[19] The distribution layer ***18*** is formed of a second conductive material which, for example, may preferably be aluminum. The distribution layer ***18*** includes a plurality of wire bonding pads at its periphery including bonding pads ***30***, ***32***, ***34***, ***36***, and ***38*** as may be seen in both **FIGS. 1** and **2**. The bonding pads ***30*** and ***38*** are electrically connected to the interconnection layer ***14*** through vias ***31*** and ***39***. The wire bonding pads ***32***, ***34***, and ***36*** are preferably similarly electrically connected to the interconnection layer ***14*** in this same manner. Such interconnections have not been illustrated in **FIG. 1** so as to not unduly complicate the figure.

[20] The integrated circuit package has a surface ***40*** upon which the substrate ***12*** is mounted in a manner known in the art. The surface ***40*** of the package ***20*** includes a plurality of wire bonding pads including pads ***42*** and ***44***. The pads ***42*** and ***44*** may be power pads or ground pads, for example. Further, the pads may be utilized for coupling to external signals such as external clock signals. The pads ***42*** and ***44*** are coupled to the wire bonding pads of the distribution layer ***18*** by wire bonds ***46*** and ***48***. As will be appreciated by those skilled in the art, the package ***20*** may include additional wire bonding pads (not shown) for being wire bonded to the other wire bonding pads of the distribution layer ***18***.

[21] **FIG. 2** shows a top view of the processed substrate ***12***. Here it may be seen that the distribution layer ***18*** is distributed essentially over the entire substrate ***12*** with distribution grids ***50***, ***52***, ***54***, ***56***, and ***58*** in essentially a star pattern. A plurality of connecting channels or vias ***60*** connect selected ones of the grids or selected portions of the grids to the interconnection layer ***14***. In this manner, power voltages and ground may be distributed to the core of the integrated circuit **22** formed in the semiconductor substrate ***12*** by the distribution layer ***18***. Other external signals such as clock signals may be similarly distributed throughout the circuit **22** in a similar manner.

[22] **FIG. 3** is a top view of another processed substrate ***72*** which embodies the present invention. Here, the distribution layer ***78*** takes the form of an orthogonal grid pattern having vias ***80*** to electrically connect respective wire bonding pads ***82*** and ***84*** to a copper interconnect pattern below (not shown) and thus to the core of the circuit formed in the substrate ***72***. The pads ***82*** and ***84*** make direct connection to the copper interconnect through vias ***92*** and ***94***, respectively. Again, the distribution layer ***78*** extends essentially across the entire area of the substrate ***72***. One of the pads, such as pad ***82*** may be coupled to a power device pad of a package to enable power to be distributed throughout the circuit formed in the substrate ***72*** and the pad ***84*** may be coupled to a ground pad of the package for distributing ground throughout the circuit formed in the substrate ***72***.

[23] In addition to the foregoing, the distribution layer ***78*** includes wire bonding pads ***100*** and ***102*** which may be utilized for connecting power and ground to I/O circuits. To this end, the distribution layer extends from the pads ***100*** and ***102*** and are coupled to the copper interconnect layer through vias ***104*** and ***106***, respectively.

[24] As may thus be seen from the foregoing, the present invention provides an integrated circuit having a distribution layer formed of, for example, aluminum, as an additional interconnect layer to deliver power to I/O cells and to the internal core of the circuit formed in an integrated circuit substrate. The aluminum distribution layer covering the substrate aids in preventing delamination of the copper interconnect layers below. Further, the distribution layer permits power and ground to be

distributed throughout the integrated circuit with greater efficiency and provides greater reliability for the overall device. The distribution layer described herein lessens the need for wider metal tracks resulting in reduced semiconductor area. Also, the distribution layer may enable a reduction in the number of copper interconnect layers required thereby decreasing processing cost and further increasing reliability. Because the distribution layer aids in precluding delamination, expensive molding compounds used for this purpose may be eliminated.

[25] While particular objects and advantages of the present invention have been shown and described in the illustrated embodiments, modifications may be made. It is therefore intended in the appended claims to cover all such changes and modifications which fall within the true spirit and scope of the invention.